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ASYNCHRONOUS RESAMPLING FOR DATA TRANSPORT

BACKGROUND OF THE INVENTION

This invention relates to the transport of a multiplex of sampled signals from one location to another, and more particularly relates to such transport accomplished asynchronously.

For the transport of a multiplex of sampled signals from one location to another, there sometimes is a premium placed on maintaining fidelity for some of the sampled signals. Conventional processing of such sampled signals typically requires the original sampling clock (or a synchronously related version) in order to convert the digital data streams back into analog form. The conventional systems thus retain crucial sample time "information" contained in the sampling clock. The signal transport is sometimes complicated by the large amount of data per signal and large number of signals which must be multiplexed. As a result, efficiency is important in order to minimize the number of additional signals and/or clocks transported.

Experience has shown that distributing the original sampling clock signals available at a first location to a distant second location (the endpoint of the data

transport) is prohibitively complex. In addition, there may be many such signals and clocks which require transport. Digital resampling of each data stream in the multiplex at the first location (onto a "suitable" clock signal, assuming a "suitable" clock signal is available) is unattractive because it results in a significant increase in word length prior to transport. Such a method is inefficient in that the amount of transported data is increased up to 50% by the resampling, if fidelity is strictly maintained. Time stamps can be imposed at the first location, but analysis shows that these are unable to provide the equivalent fidelity reconstruction available with the original sampling clock or with a resampling prior to transport, even with a significant change or improvement in the time-stamp implementation.

The present invention addresses the foregoing problems raised by conventional transport and provides alternative solutions.

BRIEF SUMMARY OF THE INVENTION

The invention is useful in a communication system for transporting a plurality of sampled signals from a first location to a second location. In such an environment, one or more data signals and a set of one or more synchronously-related clock signals exist at a first location. One or more reference signals are generated at the first location, preferably by a reference clock. At the first location, a phase signal is generated which represents at least an estimate of the difference in phase between one of the data clock signals and one of the reference signals. The one or more data signals and phase signal are transported to a second location. At the second location, resample filters are conditioned in response to the phase signal, preferably by a filter selector.

Each conditioned resample filter is responsive to the one or more data signals in order to generate one or more resampled data signals at the second location.

Digital signal processing or analog conversion may be accomplished on these one or more resampled data signals at the second location, using the second location's reference clocks, with fidelity approaching processing with the synchronous sample clocks at the first location.

By using the foregoing techniques, data may be transported between locations with a degree of economy, convenience and accuracy unavailable by using the known transport techniques. For example, the addition of the phase signal to the transport increases the transport data by less than 0.2%, while maintaining necessary fidelity provided by synchronous processing at the first location, in one application.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic block diagram of a preferred form of the present invention as operated on a single sampled signal.

Figure 2 is a schematic block diagram of one alternative of the present invention applied to a multiplicity of sampled signals.

Figure 3 is a schematic block diagram of a second, preferred, implementation of the present invention applied to a multiplicity of sampled signals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a preferred form of the present invention is used to transport a single data signal from a first location 10 to a second location 40. Within location 10, there is a source 12 of one data signal and one clock signal. More specifically, source 12 comprises a data signal source 14 and a clock signal source 16. The data signal is transmitted over an M bit bus 18, and the clock signal is transmitted over a bus 20 which also provides an input to a phase difference estimator 22. Inputs are also received by estimator 22 over a bus 26 from one or more reference clocks 24 which generate reference signals. Phase difference estimator 22 generates a phase signal on an output bus 28 representing at least an estimate of the difference in phase between the data clock signal on bus 20 and the reference clock signal on bus 26. Mux and Buffer 30 multiplexes the phase differences 28 with the data signal 18 and buffers and formats for asynchronous transport. Bus 32 comprises a long distance communication line which transports the multiplexed data signal and phase signal to location 40.

At location 40, a clock 42 transmits clock pulses over a bus 44 to a Buffer and Demux 46 and a resample filter 50 which interpolates the data received over a bus 48 from buffer 46. Clock 42 may be asynchronous with respect to other clocks shown in the system, such as data clock 16. The data is clocked out of buffer 46 by the clock signals on bus 44. Filter 50 comprises a finite impulse response (FIR) filter which interpolates based on coefficients received over an input bus 52 from a filter selector 54. Selector 54 includes a coefficient read only memory (ROM) 56 addressed by signals received over an address bus 58 from an address interface 60 which conditions

the phase signal received on bus 28 in order to address ROM 56. Buffer and Demux 46 strips off the phase estimates and provides these to the Address Interface 60 over Bus 38.

In response to the coefficients read out of ROM 56, filter 50 generates resample data signals that are transmitted over an output bus 51. Since the resampling process generates data in addition to the original M bits of data received on bus 48, the output bus 51 provides for M plus L bits of data.

Estimator 22 may comprise the phase estimate portion of part number G802480 manufactured by TRW, Inc.

Referring to Figure 2, location 100 is provided with multiple channels of multiplexed synchronously sampled data signals on a bus 106 and is provided with a high rate clock signal on a bus 108. Data is transmitted on bus 106 at a rate of 800 megabytes per second (in one embodiment), and the clock signal on bus 108 has a frequency of 800 MHz. Busses 106 and 108 provide inputs to a conventional demultiplexer 110 which separates the data and clock into individual channels, such as channels 132 and 133.

Channel 132 comprises a pair of busses 134 and 135. Bus 134 transmits M bits of data and bus 135 transmits a subharmonic of the 800 MHz clock signal. Channel 133 comprises an M bit data bus 138 and a clock bus 139 which transmits a subharmonic of the 800 MHz clock signal.

Demultiplexer 110 also extracts the frame synch signal transmitted on bus 106 from the data signals and supplies the frame synch-signal on a bus 112. Demultiplexer

110 also divides the 800 MHz clock signal to form a 50 MHz clock signal on an output conductor 114.

The frame synch signal and the 50 MHz clock signal provide inputs to a phase estimator 116 which also divides the 50 MHz clock in order to form a 2.5 MHz clock 118. Additional inputs to phase estimator 116 are provided by coherent reference clocks 120 which provide coherent (i.e., phase aligned) clock signals over buses 122 and 124. Phase estimator 116 generates a phase signal on an output conductor 126 which represents at least an estimate of the phase difference between the reference clock signals and (a) the 50 MHz clock signal and (b) the 2.5 MHz clock signal. The 2.5 MHz clock signal from clock 118 provides ambiguity resolution information for the phase difference calculation. That is, the phase signal generated on bus 126 provides a phase difference between the phase of the reference clock signals and the 2.5 MHz clock signal, but with fidelity to the least significant bits relative to the 50 MHz clock signal. By using the 2.5 MHz and the 50 MHz clock signals, the embodiment of Figure 2 can achieve a least significant bit fidelity to the phase of the 800 MHz clock signal (which is divided to form the 50 MHz clock signal).

Alternatively, rather than using the 2.5 MHz clock to resolve ambiguity, the phase estimator 116 may use the frame synch signal. In general, ambiguity resolution may be achieved by the lowest clock rate for which resampling is to occur, that is, the lowest data clock for which the resampling function is required. However, the lowest clock rate used for ambiguity resolution must be synchronous with the 800 MHz clock. Synchronization can be accomplished by dividing the 800 MHz clock by conventional dividers (not shown).

Still referring to Figure 2, a phase estimator clock signal is transmitted over a bus 128 to each of several data insertion modules, such as 130 and 131. There is one data insertion module for each of the channels of data, such as channels 132 and 133. The phase estimate signal on bus 126 also is transmitted to each of the data insertion modules. The data insertion modules insert the phase signals on buses 126 as an extra bit in the data words transmitted on the channels. As a result, output data buses 142 and 146 transmit M plus 1 bits of data. Output busses 143 and 147 continue to carry subharmonics of the 800 MHz clock signal which was passed through from busses 135 and 139.

The data and clock signals from busses 142, 143, 146 and 147 provide inputs to a packetized transport and reassemble module 150. Module 150 includes communication channels which transmit data and clock signals between location 100 and a location 160 which may be many miles from location 100.

At location 160, only one channel of data and clock signals is shown. The other channels may be processed in a manner similar to the one channel illustrated in Figure 2. The illustrated channel comprises a clock bus 162 which transmits the 800 MHz clock and a data bus 164 which transmits the M plus 1 bits received on channel 142. Bus 164 provides an input to a demultiplexer circuit 166 which separates the data into a data bus 170 of M bits and a phase estimate bus 168 which transmits the phase estimate signal to a selector 172 that may be identical to selector 54 shown in Figure 1. Coefficients are selected and provided to a resample or interpolate filter 176 over a bus 174. In the same manner described in connection with Figure 1, resample filter 176

provides resampled data signals over an output bus 180 and 800 MHz clock signals over an output bus 178.

In Figure 2, the phase estimates were multiplexed into each data signal stream by adding an extra bit to each sample. This may have advantages, in particular regarding legacy equipment. However, this does mean redundant information is included in the transport from location 100 to location 160 (since identical phase inserts are inserted multiple times). A more efficient approach is shown in Figure 3, with each phase estimate only inserted one time into the transport.

Referring to Figure 3, location 200 is provided with a multiplex of synchronously sampled data signals on a bus 206 and is provided with a high rate clock signal on a bus 208. Bus 206 transmits multiple channels of data signals at 800 megabytes per second (in one embodiment) and also transmits multiple channels of clock signals at 800 MHz over a bus 208. Buses 206 and 208 provide an input to a frame synch extract and clock divider module 210 which passes the multiple channels of data signals at 800 megabytes per second over buses 212 and passes the 800 megahertz clock signals over buses 214. Module 210 also extracts the frame synch signal from the data signals and transmits it over an output bus 218. Module 210 also divides the 800 MHz clock signal to generate a 50MHz clock signal over a bus 216.

A phase estimator 116 receives the frame synch signal and 50 MHz clock signal, and also receives coherent (e.g., phase aligned) reference clock signals from clocks 120 over input busses 122 and 124. Estimator 116 includes a 2.5 MHz clock 118. Phase estimator 116 operates in the same manner described in connection with estimator 116 shown in Figure 2 and provides a phase estimate signal over bus 126 on a

clock signal over bus 128 in the manner previously described. In general, the components of Figure 3 which bear the same numbers as components shown in Figure 2 are constructed the same and operate in the same manner described in connection with Figure 2.

As shown in Figure 3, only a single phase estimate signal on bus 126 is provided for the multiple channels of data on buses 212 and the multiple channels of clocks on busses 214.

The data and clocks on buses 212 and 214 are assembled into data packets by a packatize format and forward error correction (FEC) encode module 230. Similarly, the phase estimate signal on bus 126 and the clock on bus 128 are also assembled into data packets by module 230. All of the packets are transmitted over a communication line 232 to location 240 which may be at a distance of many miles from location 200.

At location 240, a packet to data stream assembly, FEC decode and demultiplex module 242 divides the data and clocks into multiple channels, including data channels 1-N and corresponding clock channels as shown. Only two pairs of the data and clock channels are illustrated in Figure 3. For example, in channel 1, data signals are transmitted over a data bus 244 and clock signals are transmitted over a clock bus 245. Similarly, in channel N, data signals are transmitted over a bus 248 and corresponding clock signals are transmitted over a bus 249.

The phase estimate signal is recovered by module 242 and is transmitted over a bus 252 to selectors, such as selectors 254 and 255. There is one selector for each channel (i.e., N selectors). The selectors transmit coefficients over buses 258 and 259 to resample filters 262 and 263 as shown. There is one resample filter for each

channel. As a result, there are N resample filters in total, only two of which are illustrated in Figure 3. Resample or interpolate filters 262 and 263 operate in the same manner as resample or interpolate filter 50 shown in Figure 1. As a result, resampled data signals are transmitted over buses 266 and 267, and corresponding clock signals are transmitted over buses 270 and 271.

The phase estimate signals on bus 126 must be put in packets by module 230 frequently enough to provide adequate phase estimates for selectors 254 and 255 and resample filters 262 and 263. Even at low data stream sample rates, there are, for example, greater than 50 samples of data for each phase estimate. At this point, the phase estimates are not time critical. Phase estimates may be added to the data samples with only one bit.

Referring to Figure 3, owing to the resample filters, the phase estimates on bus 252 need not be generated frequently, and there is no urgency in aligning these estimates precisely with the data bits in the high rate serial stream, such as bus 244. The phase difference information on bus 252 is not time critical (relative to the high rate serial clock on bus 245). Thus, the phase estimate need not be handled and delivered with nanosecond timing alignment to the serial data on bus 244.

Still referring to Figure 3, the phase estimate on bus 126 may be performed on a divided down clock from the 800 MHz clock signal on bus 208. The estimated phase signal on bus 126 is inserted into the high rate multiplexed data stream one signal or one packet at a time for use by the multiplex data streams at location 240. This represents the minimal processing at location 200, and the minimal amount of overhead data added to the transport, and it retains the fidelity of the clocks in locations 200 and

240. As pointed out previously, two resampler phase estimates may be needed for ambiguity resolution, one for the highest resampling clock (e.g., 50 MHz) and one for the lowest (e.g., 2.5 MHz). These two phase estimates (modulo 360°) may be combined into a single phase estimate which extends beyond 360° (i.e., resolved ambiguity). Alternatively, the frame synch signal on bus 218 may be used for ambiguity resolution.

Those skilled in the art will recognize that the preferred embodiments may be altered and modified without departing from the true spirit and scope of the invention as defined in the accompanying claims. For example, selector 54 may compute the coefficients used by filter 50.